

# Interface-dominated MIECs for integration in solid state ionic devices

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Nanoionics has become a promising field for the future development of advanced energy conversion and storage devices, such as batteries, fuel cells, and supercapacitors. For oxygen ion conductors, multilayering epitaxial thin films have been successfully proposed to tune the lattice strain subsequently increasing the ionic conductivity. Nevertheless, the implementation of this type of heterostructures still remains a challenge since it is limited to a certain number of substrates and to a lateral architecture. Therefore, clear advantages would arise if this enhancement of mass and charge transport properties could occur at intrinsic interfaces, such as grain boundaries (GBs). This will open new technological perspectives for GB-dominated MIEC materials in advanced devices such as micro-solid oxide fuel cells, lithium ion batteries or nanoionics-based resistive switching devices.

In this talk, we will detail recently published results [1,2,3] on the effect of the presence of GBs in the mass transport properties of a family of mixed ionic electronic conducting oxides,  $\text{La}_{0.8}\text{Sr}_{0.2}\text{Mn}_{1-x}\text{Co}_x\text{O}_{3+\delta}$ , in thin film form. By synthesizing a nanostructure with high density of vertically aligned GBs with high concentration of strain-induced defects, this family presents an oxygen mass transport dominated by the GB contribution in the whole range of compositions. One of the parent compounds LSM ( $x=0$ ), considered an electronic conductor in bulk, is even converted into a good mixed ionic electronic conductor by GB engineering completely changing its original nature. Moreover, during the talk we will present recent studies pointing the origin of the enhanced mass transport. The results of this study leads to fundamental insights into oxygen diffusion along GBs and to the application of these engineered nanomaterials in new advanced solid state ionic devices such are micro-solid oxide fuel cells or resistive switching memories.

## References

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